IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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SERIAL NO.: 10/585,696   ART UNIT: 2128

FILED: May 18, 2008   EXAMINER: Alhua S. A.

TITLE: PROGRAMMABLE LOGIC ARRAY FOR SCHEDULE-CONTROLLED PROCESSING

<u>Amendment A: REMARKS</u>

Upon entry of the present amendments, previous Claims 1 - 14 have been canceled and new Claims 15 - 23 substituted therefor. Reconsideration of the rejections, in light of the foregoing amendments and present remarks, is respectfully requested. The present amendments have been entered for the purpose of placing the claim language into a more proper U.S. format and for the purpose of more clearly distinguishing the present invention from the prior art.

In the Office Action, it was indicated that Claims 1 - 14 were rejected under 35 U.S.C. § 102(b) as anticipated by the Hoare publication. It was indicated that there was an objection to the use of term of "means of" in the claims. The Examiner has indicated that a certified copy of the French priority document has not been filed.

As an overview to the present reply, Applicant has revised the previous claims in the form of new Claims 15 - 23. New Claims 15 - 23 correspond, respectively, to the limitations of previous independent Claim 1, along with the limitations of dependent Claims 2 - 9. The new claims express the original limitations in a more proper U.S. format, including proper antecedent bases and proper structural interrelationships throughout. Any indefinite terminology found in the original claim language has been corrected herein.

Relative to the prior art Hoare publication, Applicant notes that the Hoare publication

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describes a discrete event simulator able to simulate only a circuit in order to check its behavior and timing. The Hoare publication includes a structure having a scheduler, a memory, a logic circuit, software and communication engines. The Hoare publication does not describe a circuit that is able to generate signals from incoming external signals and the programmable logic array with timing constraints.

In contrast, the present invention describes an integrated circuit with a programmable discrete event simulator able to generate signals from incoming signals with the same timing constraints as the programmable logic devices. In particular, and in contrast to the Hoare publication, the present invention utilizes a single clock that provides "representative signals of time units", a "synchronous programmable logic array that processes values relative the time unit", and a "scheduled times processor cooperative with the logic array so as to provide representative schedule time signals according to signals of the state change detector or by the signal programmer of the event and by the signals of the clock". Importantly, the scheduled times processor of the present invention is adapted to determine scheduled times at times delayed by the signal processor. As such, Applicant respectfully contends that independent Claim 15, reflecting the limitations of previous independent Claim 1, is not anticipated by the Hoare publication.

Relative to dependent Claim 16 corresponding to the limitations of previous dependent Claim 2, Applicant respectfully contends that the Hoare publication does not show a logic array providing "a simulator operation". The Hoare publication also fails to show that there is a time unit that is "tuned for a representation of the simulator operation".

With respect to dependent Claim 17, reflecting the limitations of previous dependent Claim 3, the Hoare publication does not show a logic array emulating at realtime a logic function without

logic emulation.

Relative to dependent Claim 19, reflecting the limitations of previous dependent Claim 5, Applicant respectfully contends that the Hoare publication does not describe "internal logic processing cells" nor "peripheral communication cells". The Hoare publication does not show the exchanging of data through a single group of lines on which is set and exchanged per time unit. The Hoare publication does not show that "the cells generate signals relative to random events or scheduled events to the schedules time processor". As such, Applicant respectfully contends that dependent Claim 19 is not anticipated by the prior art Hoare publication.

With respect to dependent Claim 20, reflecting the limitations of previous dependent Claim 6, Applicant notes that the Hoare publication does not show that the internal logic processing cells process a logic word per time unit.

Additionally, and furthermore, Applicant respectfully contends that dependent Claim 21, reflecting the limitations of previous dependent Claim 7, does not show that the internal logic processing cells are adapted to merge several data groups issued with several respective identities and to memorize each merged logic word. On this basis, Applicant contends that dependent Claim 21 is not anticipated by the Hoare publication.

With respect to the objection as to the use of the "means for" language, Applicant has removed such recitations so as to avoid the invocation 35 U.S.C. § 112, sixth paragraph.

Applicant notes the Examiner's objection that a certified copy of the French priority document has not been filed. Applicant's attorney respectfully contends that when a National Stage Application is filed, a certified copy of the corresponding French priority document would not be required. Applicant's attorney respectfully contends that the filing of a PCT application obviates the

requirement for such certified copies.

Based upon the foregoing analysis, Applicant contends that independent Claim 15 is now in proper condition for allowance. Additionally, those claims which are dependent upon independent Claim 15 should also be in condition for allowance. Reconsideration of the rejections and allowance of the claims at an early date is earnestly solicited. Since no new claims have been added above those originally paid for, no additional fee is required.

Respectfully submitted,

 March 11, 2011   /John S. Egbert/

Date

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